WHAT IS CLAIMED IS:

1. A semiconductor device for storing dual data bits with improved write/erase characteristics comprising:

a substrate defining at least one channel region separating areas of buried diffusion;

a bottom dielectric formed over said channel region and having a first edge and a second edge;

a data storage layer formed over said bottom dielectric, said data storage layer comprising a middle dielectric covering an intermediate portion of said bottom dielectric, a first floating gate extending over said bottom dielectric from said first edge to said middle dielectric and a second floating gate extending over said bottom dielectric from said second edge to said middle dielectric;

a top dielectric covering said data storage layer; and

a gate electrode formed over said top dielectric.

2. The semiconductor device of claim 1 further comprising spacers formed at the edges of said bottom dielectric, said data storage layer, said top dielectric and said gate electrode.

3. The semiconductor device of claim 1 wherein said bottom dielectric is silicon oxide.

4. The semiconductor device of claim 3 wherein said top dielectric is silicon oxide.

5. The semiconductor device of claim 3 wherein said middle dielectric is silicon nitride.

6. The semiconductor device of claim 4 wherein said middle dielectric is silicon nitride.

7. The semiconductor device of claim 3 wherein said bottom dielectric has a thickness of between about 70 and about 100 Å.

8. The semiconductor device claim 4 wherein said top dielectric has a thickness of between about 70 and about 100 Å

9. The semiconductor device of claim 5 wherein said middle dielectric has thickness of between about 50 and about 70 Å.

10. The semiconductor device of claim 1 wherein said gate electrode is a layer of poly silicon.

11. The semiconductor device of claim 1 wherein said first floating gate is made of poly silicon.

12. The semiconductor device of claim 1 wherein said second floating gate is made of poly silicon.

13. The semiconductor device of claim 1 wherein said first and second floating gates are made of poly silicon.

14. An ONO semiconductor device for storing dual data bits with improved write/erase characteristics comprising:

a substrate defining at least one channel region separating areas of buried diffusion;

a first oxide dielectric formed over said channel region and having a first edge and a second edge;

a data storage layer formed over said first oxide dielectric layer, said data storage layer comprising a nitride dielectric layer covering an intermediate portion of said first oxide dielectric layer, a first poly silicon floating gate extending over said oxide dielectric layer from said first edge to said nitride dielectric and a second poly silicon floating gate extending over said oxide dielectric layer from said second edge to said nitride dielectric;

a second oxide dielectric layer covering said data storage layer; and

a poly silicon layer formed over said second oxide dielectric layer.

15. The semiconductor device of claim 14 further comprising spacers formed at the edges of said first oxide layer, said data storage layer, said second oxide dielectric layer and said poly silicon layer.

16. The semiconductor device of claim 14 wherein said first oxide layer is silicon oxide.

17. The semiconductor device of claim 16 wherein said second oxide layer is silicon oxide.

18. The semiconductor device of claim 16 wherein said nitride dielectric is silicon nitride.

19. The semiconductor device of claim 17 wherein said nitride dielectric layer is silicon nitride.

20. The semiconductor device of claim 16 wherein said first oxide layer has a thickness of between about 70 and about 100 Å.

21. The semiconductor device of claim 17 wherein said second oxide layer has a thickness of between about 70 and about100 Å.

22. The semiconductor device of claim 18 wherein said nitride dielectric layer has thickness of between about 50 and about 70 Å.

23. A method of forming a semiconductor device for storing dual data bits with improved write/erase characteristics comprising the steps of:

providing a substrate having a multilayered dielectric layer with a bottom dielectric layer a middle dielectric layer over said bottom dielectric layer, and a top dielectric layer over said middle dielectric layer, said top dielectric layer and said middle dielectric layer having a selected pattern;

etching said middle dielectric layer, said etching step selective to said bottom and top dielectric layers such that said middle dielectric layer is "pulled back" or forms pockets between said bottom and top dielectric layers;

providing gate electrodes on the patterned top and middle dielectric layers; and

filling said pockets to form a pair of floating gates between said top and bottom dielectric layers.

24. The method of claim 23 further comprising the step of subjecting the substrate to a Rapid Thermal Process prior to said step of etching said middle dielectric layer.

25. The method of claim 23 further comprising forming an oxide on the etched surface of said etched middle dielectric layer.

26. The method of claim 23 further comprising the step of forming buried diffusion areas in said bottom dielectric layer prior to said etching step.

27. The method of claim 26 further comprising oxidizing the surface portion of said buried diffusion areas to form isolation areas between adjacent gate electrodes.

28. The method of claim 23 further comprising forming spacers on the sides of said gate electrode formed on the patterned top and middle dielectric layers.

29. The method of claim 23 further comprising the step of forming conductive word lines over said gate electrodes.

30. The method of claim 23 wherein the selected pattern of said top and middle dielectric layer is formed by providing a patterned photoresist that covers first areas and exposes second areas of said top dielectric layer, etching said top and middle dielectric layers according to said patterned photoresist.

31. The method of claim 23 wherein said bottom dielectric layer is silicon oxide.

32. The method of claim 31 wherein said top dielectric layer is silicon oxide.

33. The method of claim 31 wherein said middle dielectric layer is silicon nitride.

34. The method of claim 32 wherein said bottom dielectric layer has a thickness of between about 70Å and about 100Å.

35. The method of claim 32 wherein said top dielectric layer has a thickness of between about 70Å and about 100Å.

36. The method of claim 33 wherein said middle dielectric layer has a thickness of between about 50Å and about 70Å.

37. A method of forming an ONO semiconductor device for storing dual data bits with improved write/erase characteristics comprising the steps of:

providing a substrate having a first layer of oxide dielectric, a layer of nitride dielectric over said first layer of oxide dielectric, and a second layer of oxide dielectric over said layer of nitride dielectric, said second layer of oxide dielectric and said layer of nitride dielectric having a selected pattern;

etching said layer of nitride dielectric, said etching step selective to said first and second layers of oxide dielectric such that said nitride dielectric is "pulled back" or forms pockets between said first and second layers of oxide dielectric;

depositing a first layer of poly silicon so as to fill said pockets;

etching said first layer of poly silicon so as to expose said top surface of said first layer of oxide dielectric and to leave poly silicon floating gates in said pockets or "pull back" areas;

depositing a second layer of poly silicon over said top surface of said first and second layers of silicon oxide; and

patterning and etching said second layer of poly silicon to form a gate over said second oxide dielectric layer.

38. The method of claim 37 further comprising the step of subjecting the semiconductor substrate to a Rapid Thermal Process prior to said step of etching said layer of nitride dielectric.

39. The method of claim 37 further comprising forming an oxide on the etched surface of said etched nitride dielectric layer.

40. The method of claim 37 and further comprising the step of forming buried diffusion areas in said first layer of dielectric.

41. The method of claim 40 further comprising oxidizing the surface portion of said buried diffusion areas to form isolation areas between adjacent gate electrodes.

42. The method of claim 37 wherein the selected pattern of said second layer of oxide dielectric and said layer of nitride dielectric is formed by providing a patterned photoresist that covers first areas and second areas of said second layer of dielectric, etching said second layer of oxide dielectric and said layer of nitride dielectric according to said selected pattern.

43. The method of claim 42 further comprising the step of removing said patterned photoresist prior to said step of etching said layer of nitride dielectric.

44. The method of claim 37 further comprising forming spacers on the sides of said gate formed over said second oxide dielectric layer.

45. The method of claim 37 further comprising forming conductive word lines over said poly silicon gates.

46. The method of claim 37 wherein said first layer of oxide dielectric has a thickness of between about 70Å and about 100Å.

47. The method of claim 37 wherein said second layer of oxide dielectric has a thickness of between about 70Å and about 100Å.

48. The method of claim 37 wherein said layer of nitride dielectric has a thickness of between about 50Å and about 70Å.